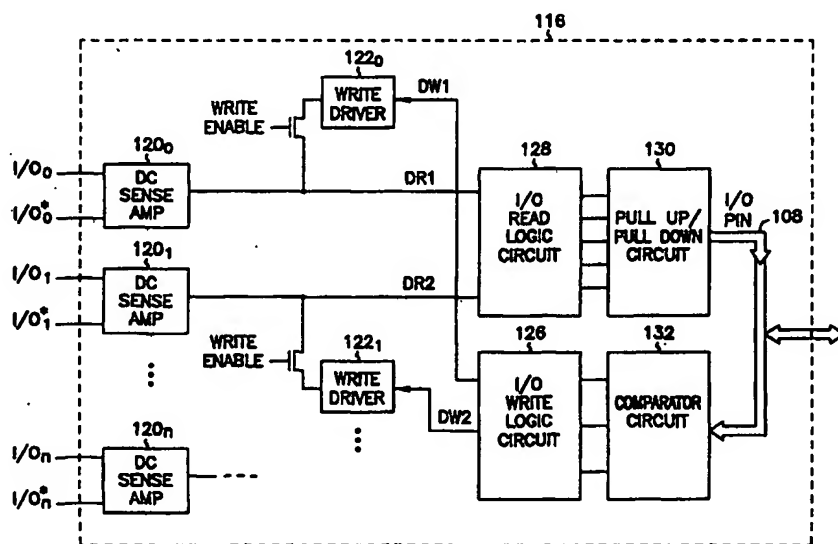




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(54) Title: MULTI-LEVEL DATA THROUGH A SINGLE INPUT/OUTPUT PIN



(57) Abstract

A method and memory circuits for increasing the data bandwidth per microprocessor operation cycle is provided. The memory circuits provide the additional bandwidth without additional input/output (I/O) pins or requiring decreased cycle times. Multiple bits of data are passed through a single input/output pin with each operation cycle. The multiple bits of data are stored in or retrieved from multiple memory cells in each cycle. The I/O pins carry analog signals which represent multiple values of binary data. This method of compressing data can be applied to any device that would benefit from the ability to transfer more data through a limited number of I/O pins.

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MULTI-LEVEL DATA THROUGH A SINGLE INPUT/OUTPUT PIN

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Field of the Invention

The present invention relates generally to semiconductor integrated circuits. More particularly, it pertains to the retrieval and storage of multi-level data through a single input/output pin.

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Background of the Invention

Modern electronic systems typically include a data storage device such as a dynamic random access memory (DRAM), static random access memory (SRAM) or other conventional memory device. The memory device stores data in vast arrays of memory cells. Each cell conventionally stores a single bit of data (a logical "1" or a logical "0") and can be individually accessed or addressed. Data is output from a memory cell during a "read" operation, and data is stored into a memory cell during a "write" operation.

In a standard read or write operation, a column decoder and a row decoder translate address signals into a single intersection of a row (wordline) and column (bitline) within the memory array. This function permits the memory cell at that location to be read from or for data to be placed into that cell. The processing of data is dependent on the time it takes to store or retrieve individual bits of data in the memory cells. Storing and retrieving the bits of data is controlled generally by a microprocessor, whereby data is passed to and from the memory array through a fixed number of input/output (I/O) lines and I/O pins. According to current digital circuit technology, each I/O pin can access, at most, one bit of data during an operation cycle. This substantially limits the potential bandwidth or speed of the memory device.

Modern applications call on electronic systems to process data at greater speeds. In order for the systems to accord these demands, the system components must increase their processing speeds. One method to increase the processing speeds is to provide additional I/O pins on the system components. However, space limitations on both microprocessor chips and memory chips preclude simply adding more and more I/O pins. Another method to increase processing speeds is to decrease the cycle time for retrieving and storing data. Upper limits for increasing cycle speeds are set by current feature size (F) of the

discrete devices from which the integrated circuit is composed. Modern photolithographic techniques, however, limit the size of the circuits that can be formed from semiconductor and other materials. At some point, the lithography cannot create a fine enough image with sufficient clarity to decrease the size of the elements of the circuit any further.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, it is desirable to develop other methods to increase the data throughput or data bandwidth without requiring an increase in I/O pins or further decrease the cycle times.

Summary of the Invention

The above mentioned problems with memory devices and other problems are addressed by the present invention and will be understood by reading and studying the following specification. A memory circuit and method of increasing the data bandwidth per cycle are described which do not require additional input/output pins or a decrease in access times.

In particular, an illustrative embodiment of the present invention includes a memory array. The memory array has multiple rows of wordlines and multiple columns of bitlines. The intersection of the multiple rows of wordlines and multiple columns of bitlines form multiple memory cells. There are a number of sense amplifiers coupled to the multiple columns of bitlines. A number of column decoders are coupled to the number of sense amps. Each column decoder can access a select number of bitlines simultaneously. There are a number of row decoders coupled to the multiple rows of wordlines. A number of input/output lines are coupled to the bitlines through the number of sense amplifiers. Also, a number of logic circuits are included which couple to a subset of the input/output lines. The logic circuits use multiple voltage levels or references to control the reading and writing to more than one memory cell simultaneously. The reading and writing operations pass multiple bits through a single input/output pin with each operation cycle.

In another embodiment, a memory circuit is provided which similarly has a memory array. The memory array has multiple rows of wordlines and multiple columns of bitlines. At the intersections of the multiple rows of wordlines and

multiple columns of bitlines are located multiple memory cells. A number of sense amplifiers are coupled to the multiple columns of bitlines. A number of column decoders couple to the number of sense amps such that a column decoder selects the output of at least two (2) sense amps. A number of row decoders
5 couple to the multiple rows of wordlines. There are a number of input/output lines coupled to the bitlines through the number of sense amplifiers. There are a number of logic circuits which have multiple inputs and outputs. Each of the logic circuits is coupled to a subset of the input/output lines. The outputs of at least one of the number of logic circuits individually couples to a number of pull-
10 up or pull-down transistors. The inputs of at least one of the number of logic circuits individually couples to a number of comparators. Each of the number of logic circuits uses multiple voltage levels to write to or read from more than one memory cell at a time.

In another embodiment, a method for writing to multiple memory cells
15 using a single input pin is provided. The method includes receiving a voltage at the pin that represents values to be stored in several memory cells. The voltage at the pin is compared with a number of distinct voltage references using a number of comparators. The output of the comparing step is coupled to a logic circuit. The method includes the logic circuit outputting bits of data to a select
20 number of input/output lines. A row in an array of memory cells is activated. The array has multiple rows of wordlines and multiple columns of bitlines. A select number of columns in the array of memory cells are activated simultaneously by a column decoder. The method further includes placing the bits of data located on the select number of input/output lines into memory cells
25 located at the intersection of the activated row and select number of activated columns. The select number of input/output lines equals the select number of columns accessed simultaneously by one column decoder.

In another embodiment, a method for reading multiple memory cells using a single output pin is provided. The method includes activating a row in
30 an array of memory cells. The array has multiple rows of wordlines and multiple columns of bitlines. The method also includes activating a select number of columns in the array of memory cells. The select number of columns are simultaneously accessed by a single column decoder. Bits of data located at the

intersection of the activated row and select number of columns are placed onto a select number of input/output lines. The select number of input/output lines are then coupled to a logic circuit. The logic circuit has a number of outputs and each output is individually coupled to a pull-up or a pull-down transistor. The
5 method further includes coupling the pull-up and pull-down transistors to a single output pin.

In another embodiment, an information handling system is provided. The information handling system includes a central processing unit and a random access memory (RAM). The RAM has a number of input/output pins. The
10 RAM has multiple rows of wordlines and multiple columns of bitlines. The RAM has a number of sense amplifiers coupled to the multiple columns of bitlines. The RAM has a column decoder coupled to the multiple columns of bitlines that accesses a select number of bitlines simultaneously. The RAM has a row decoder coupled to the multiple rows of wordlines. There are a number of
15 input/output lines coupled to the number of bitlines through sense amplifiers. A number of first logic circuits are each coupled to a select number of input/output lines. There are a number of pull-up transistors and a pull-down transistor coupled between an input/output pin and the first logic circuit for reading data out of the random access memory. A number of comparators are coupled to each
20 input/output pin and each comparator is connected to a distinct voltage reference. A second logic circuit is coupled to the number of comparators for an input/output pin. The second logic circuit couples to a select number of input/output lines at any one time for writing data into the random access memory. A system bus communicatively couples to the central processing unit
25 and the RAM.

This invention enables an electronic system with a memory circuit to have a greater data bandwidth or speed without increasing the number of input/output pins or decreasing the access time of the part. It is advantageous over increasing the input/output pin count because it uses much less die area for
30 the bond pad area and possibly less area for signal routing. The implementation of the present invention will enable memory circuits to operate faster without having to resize the transistors, change the memory addressing sequence, change the operating voltage, or using other methods for increasing the overall speed of

microprocessors. This method of compressing data can be applied to any device that would benefit from the ability to transfer more data through a limited number of I/O pins.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figure 1 is a block diagram illustrating an memory circuit according to the teachings of the present invention.

Figure 2 is a block diagram illustrating in more detail the array of memory cells, the row and column decoders, and the input/output (I/O) control circuit of the memory circuit of Figure 1.

Figure 3 is a block diagram illustrating in more detail the (I/O) control circuit portion of the memory circuit of Figure 1.

Figure 4A is a boolean logic circuit illustrating in more detail an embodiment of the I/O read logic portion of the I/O control circuit of Figure 3.

Figure 4B is a schematic diagram illustrating in more detail an embodiment of the pull-up/pull-down portion of the I/O control circuit of Figure 3.

Figure 4C is a truth table illustrating the inputs and outputs according to the embodiment of the logic circuit in Figure 4A.

Figure 5A is a schematic diagram illustrating in more detail an embodiment of the comparator circuit portion of the I/O control circuit of Figure 3.

Figure 5B is a boolean logic circuit illustrating in more detail an embodiment of the I/O write logic circuit portion of the I/O control circuit of Figure 3.

Figure 5C is a truth table illustrating the inputs and outputs according to the embodiment of the logic circuit in Figure 5B.

Figure 6 is a block diagram illustrating an information handling system according to an embodiment of the present invention.

Description of the Embodiments

In the following detailed description of the invention, reference is made
5 to the accompanying drawings which form a part hereof, and in which is shown,
by way of illustration, specific embodiments in which the invention may be
practiced. In the drawings, like numerals describe substantially similar
components throughout the several views. These embodiments are described in
sufficient detail to enable those skilled in the art to practice the invention. Other
10 embodiments may be utilized and structural, logical, and electrical changes may
be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include
any structure having an exposed surface with which to form the integrated circuit
(IC) structure of the invention. The term substrate is understood to include
15 semiconductor wafers. The term substrate is also used to refer to semiconductor
structures during processing, and may include other layers that have been
fabricated thereupon. Both wafer and substrate include doped and undoped
semiconductors, epitaxial semiconductor layers supported by a base
semiconductor or insulator, as well as other semiconductor structures well
20 known to one skilled in the art. The term conductor is understood to include
semiconductors, and the term insulator is defined to include any material that is
less electrically conductive than the materials referred to as conductors. The
following detailed description is, therefore, not to be taken in a limiting sense,
and the scope of the present invention is defined only by the appended claims,
25 along with the full scope of equivalents to which such claims are entitled.

Figure 1 is a block diagram illustrating an electronic circuit according to
the teachings of the present invention.

Figure 1 includes a memory array 110. The memory array 110 is coupled
to a sense amplifier block 111. The sense amplifier block is coupled to a column
30 decoder block 112. The memory array 110 is coupled to a row decoder block
114. The column decoder block 112 is additionally coupled to an input/output
(I/O) control circuit block 116.

Figure 1 further includes an electronic system 102. The electronic system 102 couples through a control bus 104 to a control circuit 118. The control circuit 118 couples to the row decoder block 114, the sense amplifier block 111, the column decoder block 112 and the input/output control circuit block 116. The I/O control circuit block 116 additionally includes a grouping of a number of input/output pins 108 which couple to the electronic system 102. The electronic system 102 further includes an address bus 106 that couples to the row decoder block 114 and the column decoder block 112. The control circuit 118, the row decoder block 114, the memory array 110, the sense amplifier block 111, the column decoder block 112 and the I/O control circuit block 116 all form a part of memory device 100.

Figure 2 is a block diagram illustrating in more detail a portion of the memory device 100. Memory array 110 includes multiple rows of wordlines, WL_1, WL_2, \dots, WL_n , and multiple columns of bitlines, BL_0, BL_1, \dots, BL_n . The intersection of the multiple rows of wordlines, WL_1, WL_2, \dots, WL_n , and multiple columns of bitlines, BL_0, BL_1, \dots, BL_n , form multiple memory cells 105₁-105_n. The sense amplifier block 111 comprises a number of sense amplifiers, 111₀, 111₁, \dots , 111_n, which couple to the multiple columns of bitlines. The column decoder block 112 comprises a number of column decoders coupled to the number of sense amplifiers 111₀, 111₁, \dots , 111_n. Each column decoder accesses a select number of bitlines simultaneously. The row decoder block 114 includes a number of row decoders which couple to the multiple rows of wordlines. A number of input/output lines, $I/O_0, I/O_1, \dots, I/O_n$, couple to the number of bitlines through the number of sense amplifiers. An address bus 106 couples to both the row decoder block 114 and the column decoder block 112. The number of input/output lines couple to the I/O control circuit block 116 and a number of I/O pins 108 couple to the I/O control circuit block.

Figure 3 is a block diagram illustrating in more detail a portion of the I/O control circuit block 116 of the electronic circuit of Figure 1. In Figure 3, a number of input/output lines, $I/O_0, I/O_1, \dots, I/O_n$, and their complementary pairs are coupled to a number of DC sense amplifiers, 120₀, 120₁, \dots , 120_n. The input/output lines, $I/O_0, I/O_1, \dots, I/O_n$, couple from the DC sense amplifier to a

write enable pass transistor and into an input/output (I/O) read logic circuit 128. When the write enable pass transistor is deactivated, the number of input/output lines couple only to the I/O read logic circuit 128. The I/O read logic circuit 128 has multiple inputs and outputs. The outputs of the I/O read logic circuit 128 couple to a pull-up/pull-down circuit 130. The pull-up/pull-down circuit 130 couples to and delivers an analog output to a single input/output (I/O) pin 108. In any given "read" operation cycle, at least two pairs of complementary input/output lines have deactivated write enable pass transistors and directly input simultaneously into the I/O read logic circuit 128. In this embodiment, a single I/O pin 108 reads from at least two memory cells simultaneously. In an alternative embodiment, a single I/O pin reads from at least four memory cells simultaneously.

Conversely, when the write enable pass transistors are activated, the input/output lines, $I/O_0, I/O_1, \dots, I/O_n$, couple through a write driver shown in Figure 3 as 122₀ and 122₁. The write driver, 122₀ and 122₁ respectively, receives the output of an I/O write logic circuit 126. The I/O write logic circuit 126 receives a number of inputs from a comparator circuit 132. The comparator circuit 132 receives an input from a single I/O pin 108. In any given "write" operation cycle, at least two write enable pass transistors are activated simultaneously such that the output of the I/O write logic circuit 126 is coupled to at least two sets of input/output lines. This allows for a single I/O pin 108 to write to at least two memory cells simultaneously. In an alternative embodiment, a single I/O pin writes to at least four memory cells simultaneously.

Figure 4A provides a Boolean logic circuit 140 which exemplifies in more detail an embodiment of the I/O read logic circuit 128 of the I/O control circuit block 116 of Figure 3. In this embodiment, two input/output (I/O) lines, DR1 and DR2 respectively, couple to the I/O read logic circuit 128. The Boolean logic circuit 140 includes a NOR gate 142 outputting to a pull-down gate. The Boolean logic circuit 140 further includes a series of AND gates 144, 146 and 148 respectively. The output of AND gate 144 couples to a pull-up transistor. The output of AND gate 146 couples to a second pull-up transistor, and the output of AND gate 148 couples to a third pull-up transistor.

Figure 4B provides a pull-up/pull-down circuit 150 which exemplifies, in more detail, an embodiment of the pull-up/pull-down circuit 130 of the I/O control circuit block 116. The pull-up/pull-down circuit 150 includes a number of pull-up and pull-down transistors. In the embodiment, a pull-up transistor 154 is coupled to a voltage level of V_{dd} . A pull-up transistor 156 is coupled to a voltage level of one-third ($1/3$) V_{dd} . A pull-up transistor 158 is coupled to a voltage level of two-thirds ($2/3$) V_{dd} . Further, a pull-down transistor 152 is coupled to ground. The pull-up and pull-down transistors, 152, 154, 156, and 158 respectively, are collectively coupled to a single input/output (I/O) pin 159. In this embodiment, the number of pull-up and pull-down transistors output a single analog signal through a single I/O pin.

Figure 4C is a truth table illustrating the inputs and outputs according to the embodiment of the Boolean logic circuit 140, illustrated in Figure 4A. As illustrated, the four logical combinations for DR1 and DR2 each activate one of the transistors of pull-up/pull-down circuit 150. The selected transistor either pulls the I/O pin 159 up to its associated supply voltage, or down to ground. This analog voltage indicates the values stored in the multiple cells that are read simultaneously.

Figure 5A provides a comparator circuit 160 which exemplifies, in more detail, an embodiment of the comparator circuit 132 of the I/O control circuit 116 of Figure 3. In this embodiment, comparator circuit 160 receives an input through a single I/O pin 168. I/O pin 168 may be one in the same with I/O pin 159 above. The I/O pin 168 carries an analog signal. The I/O pin 168 couples to a number of comparators, 162, 164, 166 respectively. Each comparator, 162, 164, and 166 respectively, couples to a different voltage reference level. Comparator 166 couples to a voltage reference level of V_{dd} . Comparator 164 couples to a voltage level reference of two-thirds ($2/3$) V_{dd} . Comparator 162 couples to a voltage level reference of one-third ($1/3$) V_{dd} .

Figure 5B provides a Boolean logic circuit 170 illustrating in more detail an embodiment of the I/O write logic circuit 126 of the I/O control circuit 116 of Figure 3. In this embodiment, Boolean logic circuit 170 includes a pair of OR gates, 172 and 174 respectively. The Boolean logic circuit 170 receives multiple inputs from the embodiment of the comparator circuit 160. The Boolean logic

circuit 170 outputs to I/O lines DW1 and DW2. The I/O lines, DW1 and DW2, carry digital signals. The output of the V_{dd} comparator and the two-thirds (2/3) V_{dd} comparator are input to OR gate 172 of the Boolean logic circuit 170. The output of the V_{dd} comparator and the one-third (1/3) V_{dd} comparator are input
5 into OR gate 174.

Figure 5C is a truth table illustrating the inputs and outputs according to the embodiment of Boolean logic circuit 170 illustrated in Figure 5B. As illustrated, the four logical combinations for DW1 and DW2 each result from the output of a pair of comparators of comparator circuit 160. The output of the
10 comparators route the analog signal received from the I/O pin 168 to the Boolean logic circuit 170. The Boolean logic circuit 170 translates the values represented by the analog signal into bits of digital data for storage in multiple cells simultaneously.

Method of Operation

15 In operation, the method of writing to multiple memory cells, within memory array 110, includes receiving an analog voltage at a single input/output (I/O) pin 108. The voltage received at the pin 108 represents at least two (2) binary values to be stored in multiple memory cells. The voltage received at the I/O pin 108 is input to a comparator circuit 132. The comparator circuit 132
20 includes an exemplary embodiment, such as comparator circuit 160. The comparator circuit 160 includes a number of comparators, 162, 164, and 166 respectively. The voltage input, received at I/O pin 108, is compared with a number of distinct voltage references using comparators, 162, 164, and 166 respectively. The distinct voltage references include V_{dd} , two-thirds (2/3) V_{dd} ,
25 and one-third (1/3) V_{dd} . The output of comparator circuit 160 is coupled to an I/O write logic circuit 126. The I/O write logic circuit 126 includes an embodiment of Boolean logic circuit 170. Boolean logic circuit 170 outputs to a select number of input/output lines. The select number of I/O lines, equals at least two, DW1 and DW2 respectively. A row (wordline) within the memory
30 array 110 is activated. A select number of columns within the memory array 110 are activated by the column decoder 112, e.g., two columns. The bits of data located on the select number of input/output lines, DW1 and DW2 respectively, are placed into individual memory cells, within the array 110, which are located

at the intersection of the activated row and select number of activated columns. In one embodiment, the select number of input/output lines, DW1 and DW2 respectively, equals the select number of columns accessed simultaneously by the column decoder 112.

5 In the read operation, the method includes activating a row (wordline) in a memory array 110. Column decoder 112 activates a select number of columns of bitlines in the memory array 110. Bits of digital data, located at the intersection of the activated row and select number of columns, are placed onto a select number of input/output lines. In one embodiment, the bits of data are
10 placed on at least two (2) I/O lines, DR1 and DR2 respectively. The select number of I/O lines are coupled to an I/O read logic circuit 128 wherein the I/O read logic circuit 128 has a number of outputs. The number of I/O lines coupling to an embodiment of the I/O read logic circuit 128 carry bits of digital data into the I/O read logic circuit 128. Each output of the I/O read logic circuit 128 is
15 coupled to a pull-up/pull-down circuit 130. The I/O read logic circuit 128 includes the embodiment of Boolean logic circuit 140. The Boolean logic circuit 140 includes NOR gate 142, AND gate 144, AND gate 146, and AND gate 148. Each of the gates, 142, 144, 146, and 148 respectively, have outputs such that each output is individually coupled to a pull-up or pull-down transistor within
20 pull-up/pull-down circuit 130. The pull-up/pull-down circuit 130 includes a pull-down transistor 152, a pull-up transistor 154, a pull-up transistor 156, and a pull-up transistor 158. The number of pull-up and pull-down transistors in pull-up/pull-down circuit 130 couple to multiple voltage levels. The number of pull-up and pull-down transistors in pull-up/pull-down circuit 130 couple an analog
25 signal to a single input/output pin 159.

Figure 6 is a block diagram illustrating an information handling system 600 according to an embodiment of the present invention. The information handling system includes a central processing unit 604. The central processing unit is coupled to a random access memory (RAM) 630 by a system bus 610.
30 The RAM can be constructed as the memory device 100 shown in the previous Figures.

Conclusion

It is to be understood that the above description is intended to be illustrative, and not restrictive. Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the present invention. The scope of the invention should be determined with reference to the appended claims along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A memory circuit having a number of input/output pins, the memory circuit comprising:
 - 5 a memory array, the memory array having multiple rows of wordlines and multiple columns of bitlines, the intersection of the multiple rows of wordlines and multiple columns of bitlines comprising multiple memory cells;
a number of sense amplifiers coupled to the multiple columns of bitlines;
a column decoder coupled to the number of sense amplifiers, wherein the
10 column decoder accesses a select number of bitlines simultaneously;
a row decoder coupled to the multiple rows of wordlines;
a number of input/output lines coupled to the number of bitlines through the number of sense amplifiers; and
a number of logic circuits that are each coupled to a subset of the
15 input/output lines, wherein the logic circuit uses multiple voltage levels to control writing to more than one memory cell or to control reading from more than one memory cell using a single input/output pin.
2. The memory circuit of claim 1, wherein the single input/output pin reads
20 or writes to at least two (2) memory cells simultaneously.
3. The memory circuit of claim 1, wherein the single input/output pin reads or writes to at least four (4) memory cells simultaneously.
- 25 4. The memory circuit of claim 1, wherein the number of logic circuits use voltage levels of zero (0), one-third (1/3), two-thirds (2/3) and one (1) V_{dd} to distinguish binary states for two memory cells using the single input/output pin.
5. The memory circuit of claim 1, wherein the number of logic circuits
30 comprise multiple inputs and outputs, and wherein the outputs of at least one of the number of logic circuits each individually couple to a pull-up or pull-down transistor for reading data from the number of memory cells.

6. The memory circuit of claim 1, wherein the number of logic circuits comprise multiple inputs and outputs, and wherein the inputs of at least one of the number of logic circuits each individually couple to a comparator for writing data into the number of memory cells.
- 5
7. The memory circuit of claim 1, wherein the number of logic circuits comprise a number of outputs, the number of outputs coupled to a number of pull-up devices, and the pull-up devices are coupled to different voltage levels.
- 10 8. The memory circuit of claim 7, wherein the number of pull-up devices are coupled to individual voltage references of one-third ($1/3$), two-thirds ($2/3$) and one (1) V_{dd} .
9. The memory circuit of claim 1, wherein the number of logic circuits
15 comprise a number of inputs, the number of inputs coupled to a number of comparators, and the comparators are coupled to different voltage references.
10. The memory circuit of claim 9, wherein the number of comparators are coupled to individual voltage references of one-third ($1/3$), two-thirds ($2/3$) and
20 one (1) V_{dd} .
11. A memory circuit, comprising:
a memory array, the memory array having multiple rows of wordlines and multiple columns of bitlines, the intersection of the multiple rows of
25 wordlines and multiple columns of bitlines comprising multiple memory cells;
a number of sense amplifiers coupled to the multiple columns of bitlines;
a column decoder coupled to the number of sense amplifiers, wherein the column decoder selects the output of at least two (2) sense amplifiers;
a row decoder coupled to the multiple rows of wordlines;
30 a number of input/output lines coupled to the number of bitlines through the number of sense amplifiers; and
a number of logic circuits having multiple inputs and outputs and each coupled to a subset of the input/output lines, the outputs of at least one of the

number of logic circuits individually couple to a number of pull-up or pull-down transistors, the inputs of at least one of the number of logic circuits individually couple to a number of comparators, and wherein the number of logic circuits use multiple voltage levels to write to or read from more than one memory cell.

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12. The memory circuit of claim 11, wherein the multiple voltage levels are zero (0), one-third (1/3), two-thirds (2/3) and one (1) V_{dd} .

13. The memory circuit of claim 11, wherein the number of comparators
10 couple to a single input/output pin.

14. The memory circuit of claim 11, wherein the number of pull-up and pull-down transistors output an analog signal to a single input/output pin.

15 15. The memory circuit of claim 11, wherein the number of input/output lines carry digital signals.

16. A method for writing to multiple memory cells using a single input pin, the method comprising:

20 receiving a voltage at the pin that represents values to be stored in multiple memory cells;

comparing the voltage at the pin with a number of distinct voltage references using a number of comparators;

25 coupling the output of the comparators to a logic circuit, wherein the logic circuit outputs to a select number of input/output lines;

activating a row in an array of memory cells, the array having multiple rows of wordlines and multiple columns of bitlines;

30 activating a select number of columns in the array of memory cells, wherein the select number of columns are simultaneously accessed by a column decoder; and

placing the bits of data located on the select number of input/output lines into the memory cells located at the intersection of the activated row and select number of activated columns, wherein the select number of input/output lines

equals the select number of columns accessed simultaneously by one column decoder.

17. The method of claim 16, wherein comparing the voltage at the pin
5 comprises comparing the voltage to zero (0), one-third (1/3), two-thirds (2/3) and one (1) V_{dd} .

18. The method of claim 16, wherein receiving a voltage at the pin comprises receiving an analog signal that represents at least two (2) binary values.

10

19. The method of claim 16, where activating the select number of columns comprises activating at least two (2) columns.

20. A method for reading multiple memory cells using a single output pin,
15 the method comprising:

activating a row in an array of memory cells, the array having multiple rows of wordlines and multiple columns of bitlines;

activating a select number of columns in the array of memory cells,
wherein the select number of columns are simultaneously accessed by a single
20 column decoder;

placing the bits of data located at the intersection of the activated row and select number of columns onto a select number of input/output lines;

coupling the select number of input/output lines to a logic circuit,
wherein the logic circuit has a number of outputs, each output is individually
25 coupled to a pull-up or a pull-down transistor; and

coupling the pull-up and pull-down transistors to a single output pin.

21. The method of claim 20, wherein coupling the pull-up and pull-down transistors to the output pin places an analog signal on the output pin.

30

22. The method of claim 20, wherein coupling the input/output lines to a logic circuit comprises coupling bits of digital data into the logic circuit.

23. The method of claim 20, where activating a select number of columns comprises at least two (2) columns.

24. An information handling system comprising:

5 a central processing unit;

a random access memory, the random access memory having a number of input/output pins and further comprising:

multiple rows of wordlines and multiple columns of bitlines;

10 a number of sense amplifiers coupled to the multiple columns of bitlines;

a column decoder coupled to the multiple columns of bitlines that accesses a select number of bitlines simultaneously;

a row decoder coupled to the multiple rows of wordlines;

15 a number of input/output lines coupled to the number of bitlines through the sense amplifiers;

a number of first logic circuits, each circuit coupled to a select number of input/output lines;

20 for each first logic circuit, a number of pull-up transistors and a pull-down transistor coupled between an input/output pin and the first logic circuit for reading data out of the random access memory;

a number of comparators coupled to each input/output pin, wherein each comparator is connected to a distinct voltage reference; and

25 a second logic circuit coupled to the number of comparators associated with a respective input/output pin;

input/output lines at any one time writing data into the random access memory; and

30 a system bus for communicatively coupling the central processing unit and the random access memory.

25. The information handling system of claim 24, wherein the select number of bitlines simultaneously accessed by the column decoder is equal to or greater than two (2).

5 26. The information handling system of claim 24, wherein the input/output pin carries an analog signal.

27. The information handling system of claim 24, wherein the input/output lines carry digital signals.

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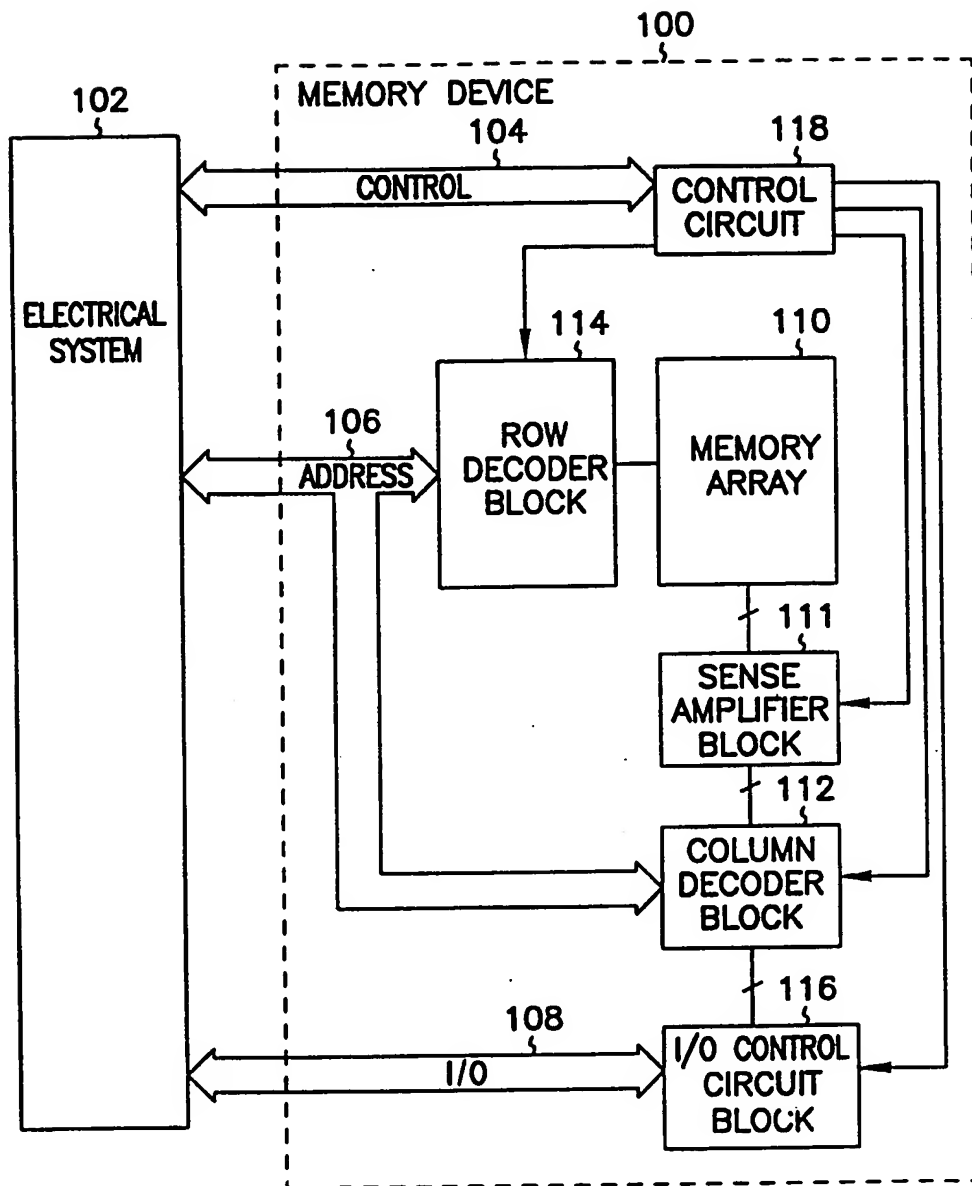


FIG. 1

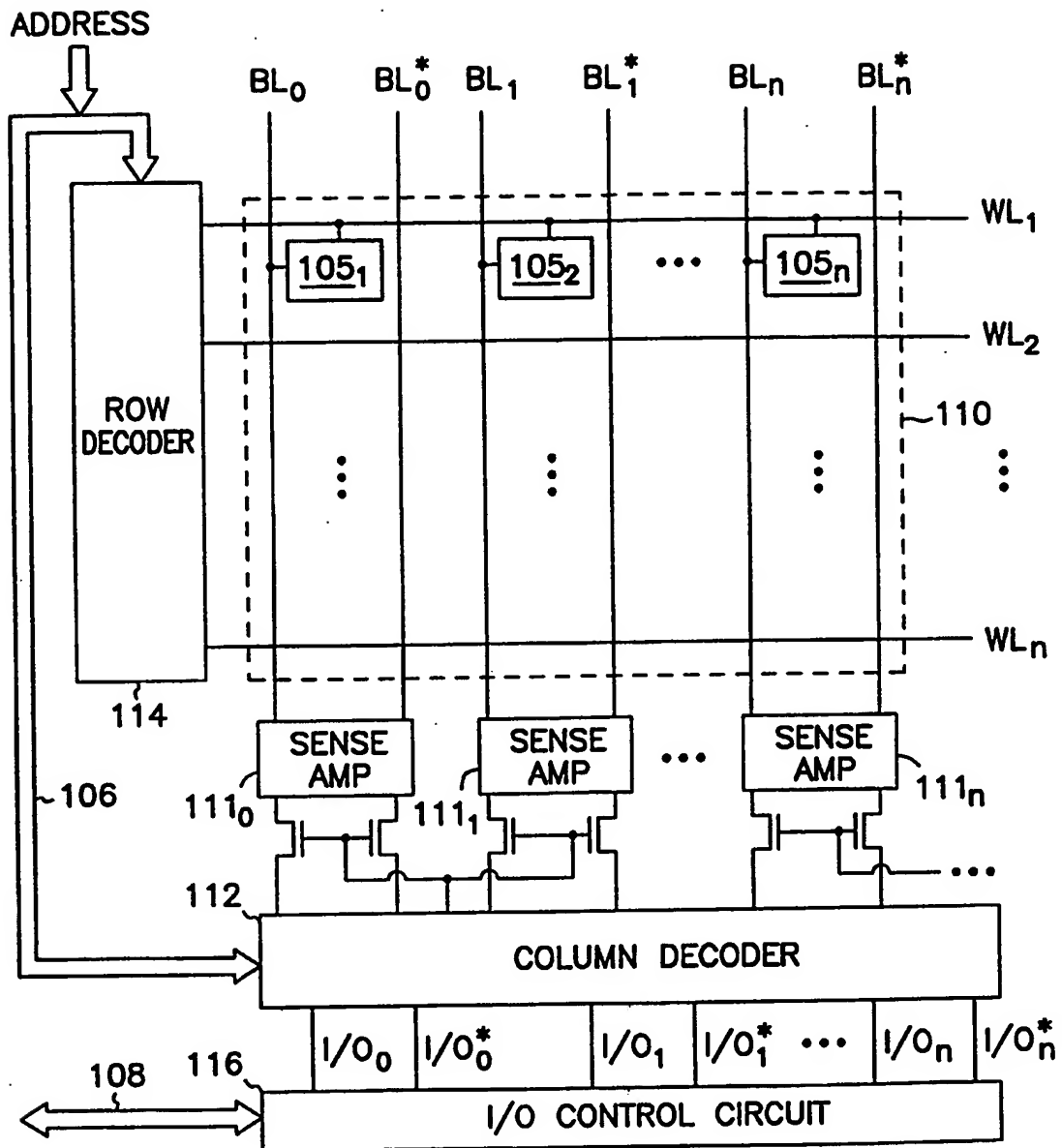
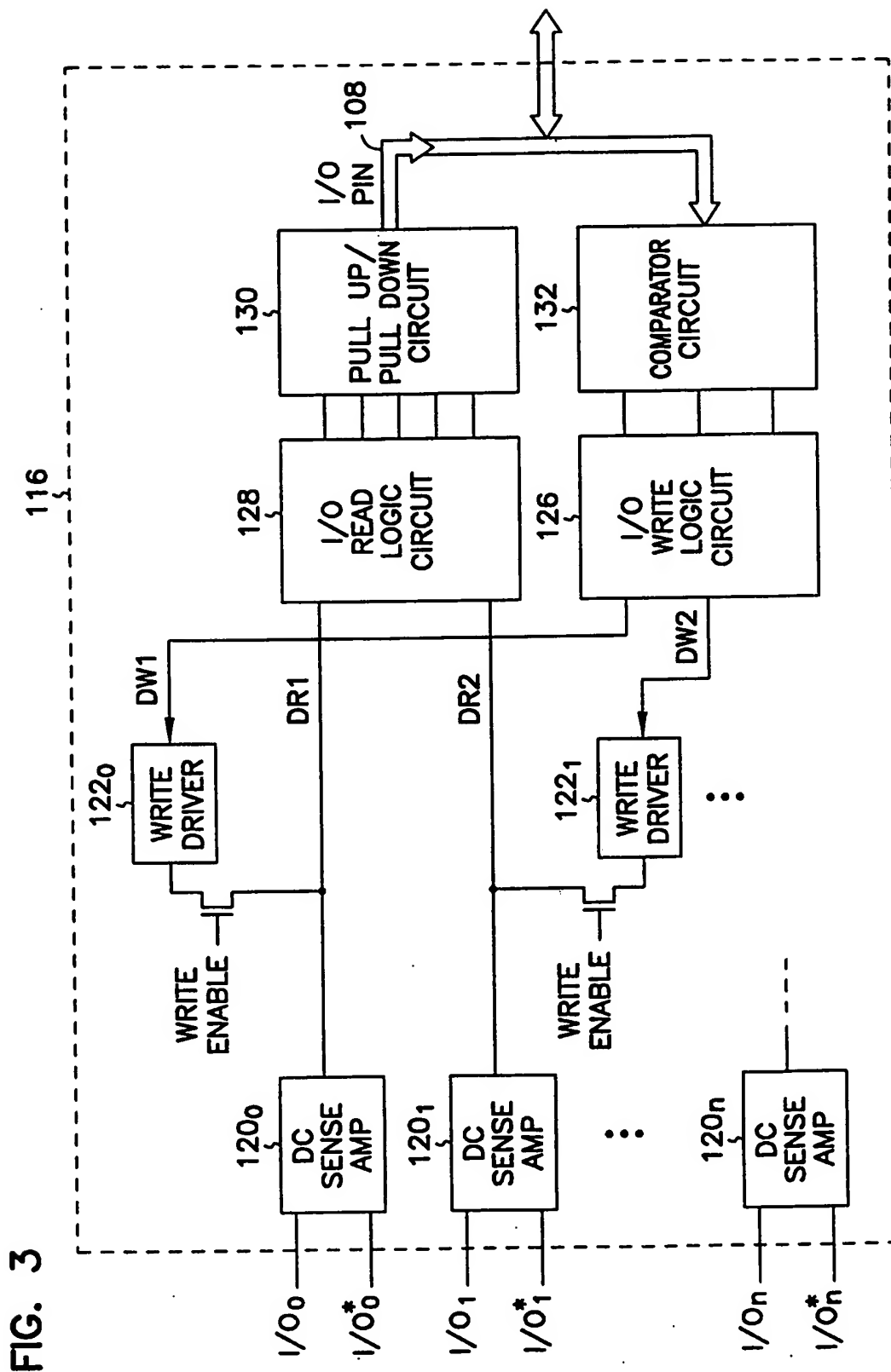


FIG. 2



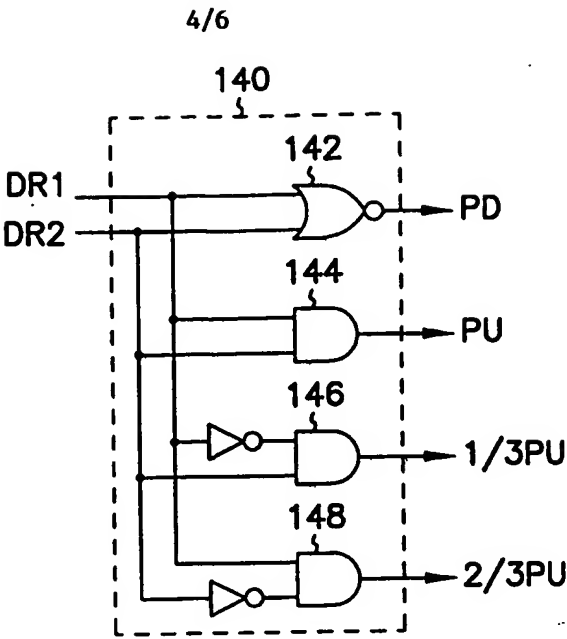


FIG. 4A

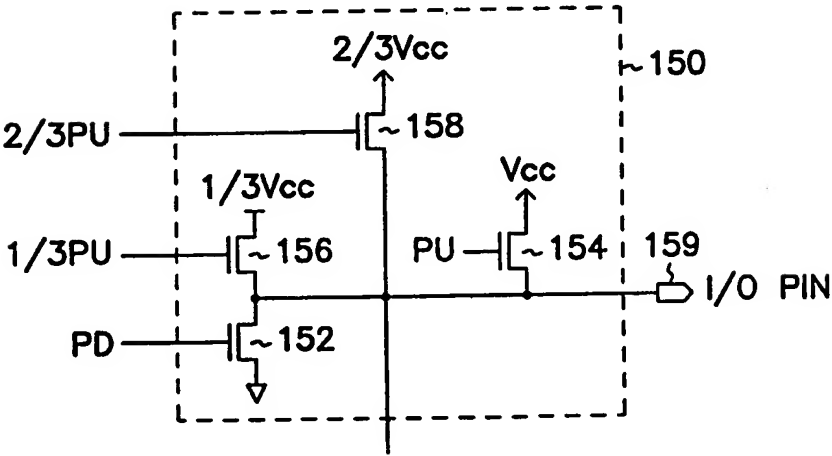


FIG. 4B

DR1	DR2	PD	1/3PU	2/3PU	PU
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

FIG. 4C

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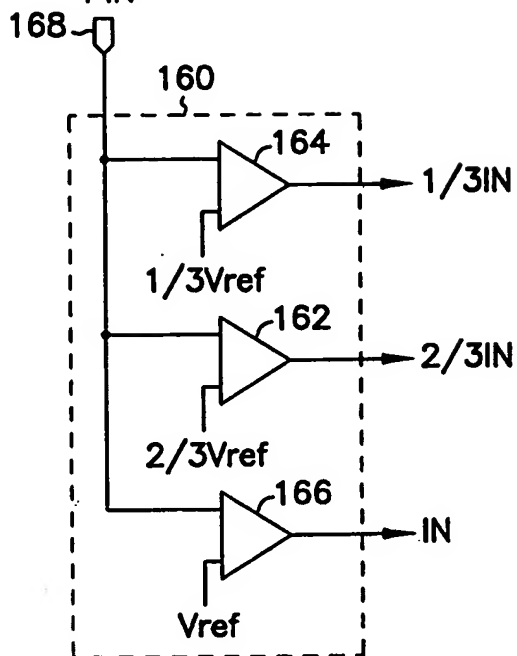
INPUT/OUTPUT
PIN

FIG. 5A

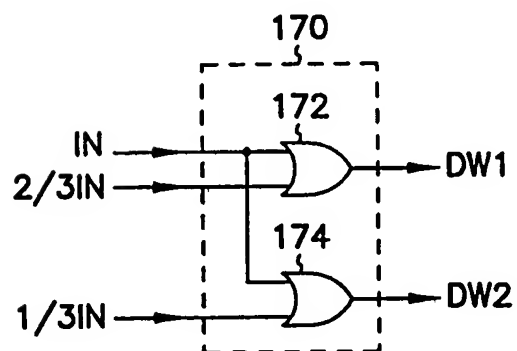


FIG. 5B

IN	$2/3IN$	$1/3IN$	DW1	DW2
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
1	0	0	1	1

FIG. 5C

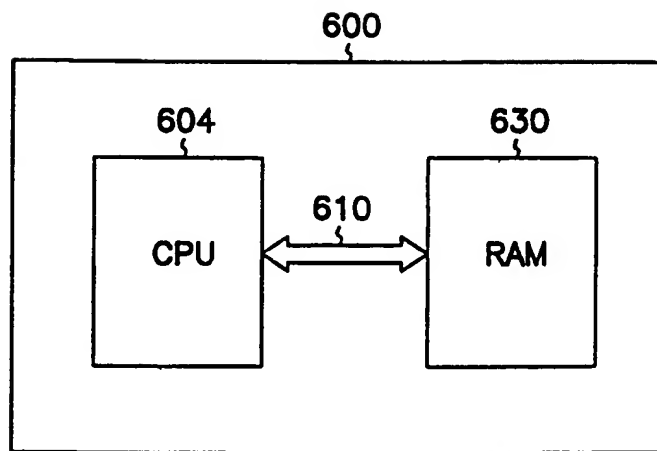


FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 99/03822

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G11C7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GB 2 253 078 A (RADAMEC GROUP PLC) 26 August 1992 see page 3, line 20 - page 4, line 12; figure 2	1
A	US 5 675 336 A (HAKKARAINEN JUKA MIKKO) 7 October 1997 see the whole document	1-3, 20-22
A	DE 41 35 220 C (SMART DISKETTE GMBH) 8 April 1993 see column 2, line 63 - column 3, line 61	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"A" document member of the same patent family

Date of the actual completion of the international search

10 June 1999

Date of mailing of the international search report

21/06/1999

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Degraeve, L

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 99/03822

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2253078	A	26-08-1992	NONE
US 5675336	A	07-10-1997	NONE
DE 4135220	C	08-04-1993	AU 2691592 A 21-05-1993 WO 9308572 A 29-04-1993